Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in this application--including previously cancelled claims 66, 68-69, previously withdrawn claims 25-65 and 70-81, and currently amended claims 1, 3-11, 15-19, and 82-83.

Listing of Claims:

Claim 1 (currently amended): A semiconductor device comprising:

a layer of semiconductor material;

a thyristor formed in the layer of semiconductor material;

the thyristor comprising PNPN sequential regions in the layer of semiconductor material for anode, N-base, P-base and cathode regions respectively, in which

a first ~~at least one~~ base-emitter junction region is defined between the N-base region and the anode region,

a second base-emitter junction region is defined between the P-base region and the cathode region, and

a base-to-base junction region is defined between the N-base region and the P-base region; and

leakage species disposed in a region of the semiconductor material ~~and~~ that extends across ~~the~~ at least one of the first and the second base-emitter junction regions while remaining substantially clear of the base-to-base junction region.

Claim 2 (original): The device of claim 1, in which the leakage species comprises carbon.

Claim 3 (currently amended): The device of claim 2, in which the carbon comprises a density across the at least one of the first and the second base-emitter junction regions sufficient to establish a low-voltage leakage characteristic therefor ~~the at least one base-emitter junction~~ that is substantially greater than ~~the leakage therefor~~ that which would otherwise be available therefor absent the carbon.

Claim 4 (currently amended): The device of claim 3, the low-voltage leakage characteristic greater than twice the leakage which would otherwise be available therefor absent the carbon.

Claim 5 (currently amended): The device of claim 3, in which the low-voltage, leakage characteristic is characterized ~~across~~ to a bias ~~region~~ condition of less than 0.50 volts.

Claim 6 (currently amended): The device of claim 2, in which:

~~the at lease one base-emitter junction is defined between an anode and N-base of the thyristor;~~

the layer of semiconductor material conductor material is defined at least in part by a layer of silicon over an insulator of an SOI structure;

the anode region and the N-base region are formed in ~~a~~ the layer of silicon ~~of an SOI substrate~~;

the N-base region defines ~~comprises~~ an area per a planar top view of the layer of silicon of magnitude less than 100 x 200 nm^2; and

the carbon is implanted in the layer of silicon with patterning to defines a boundary in the layer of silicon, the boundary ~~short~~ for the carbon implants disposed substantially clear of the base-to-base junction region ~~between the N-base and the P-base of the thyristor~~.

Claim 7 (currently amended): The device of claim 2, ~~further comprising:~~ in which

the layer of semiconductor material comprises a layer of silicon disposed over insulator of an SOI structure;

each of the ~~thyristor comprising~~ N-P-N-P ~~doped~~ regions for the thyristor are formed in the layer of silicon for the respective cathode, P-base, N-base and anode regions ~~of the thyristor~~; and

each of the first and the second base-emitter junction regions ~~for the respective anode-to-N-base and cathode-to-P-base boundaries comprising~~ comprise carbon-

silicon type defects for at least part of the leakage species for effecting low-level leakage.

Claim 8 (currently amended): The device of claim 2, in which the density of the carbon within the at least one of the first and the second base-emitter junction regions is sufficient to reduce ~~the~~ a gain ~~of a respective one of~~ for the bipolar ~~transistor for the thyristor over a~~ device defined in part by the junction region when it is characterized at a given low-bias ~~range therefor~~ condition.

Claim 9 (currently amended): The device of claim 8, in which the ~~density of the~~ carbon ~~and an annealed structure therefor~~ is formed within the at least one of the first and the second base-emitter junction regions for an anneal structure and density ~~are~~ sufficient to ~~establish~~ reduce the gain ~~of the respective~~ for the bipolar ~~transistor~~ device to a magnitude less than one-half a gain that would otherwise be available therefore absent the carbon.

Claim 10 (currently amended): The device of claim 8, in which the at least one of the base-emitter junction regions comprises a depletion width and the density of the carbon in the depletion width is greater than 10^{17} per ~~(cm)^3 in the depletion width and less than 10^{16} per (cm)^3 across the base-base junction~~.

Claim 11 (currently amended): A thyristor-based memory device, comprising:

a thyristor formed in semiconductor material, the thyristor comprising:

an anode/cathode,

a cathode/anode,

first and second base regions disposed between the anode/cathode and the cathode/anode,

a first base-emitter junction region defined between the anode/cathode and the first base region,

a second base-emitter junction region defined between the cathode/anode and the second base;

a base-to-base junction region defined between the first and the second base regions; and

lifetime-adjusting defects disposed within a region of the semiconductor material that includes at least a portion of a depletion region of the first base-emitter junction, the region of the lifetime-adjusting defects remaining substantially clear of the base-to-base junction region.

Claim 12 (original): The device of claim 11, the lifetime-adjusting defects comprising carbon-type defects.

Claim 13 (original): The device of claim 12, in which the carbon-type defects comprise an average diameter less than a nanometer.

Claim 14 (original): The device of claim 12, in which the carbon-type defects are formed by an anneal of the semiconductor material for the first base-emitter junction region with carbon disposed therein.

Claim 15 (currently amended): The device, of claim 14, the carbon-type defects comprising a density for the carbon, and formed by an anneal, sufficient to import non-ideal I-V characteristics for the junction in at least a low voltage bias ~~region~~ condition ~~therefor~~.

Claim 16 (currently amended): The device of claim 12, in which each of the first and the second base-emitter junction regions of the thyristor comprises carbon-type defects as the lifetime-adjusting defects.

Claim 17 (currently amended): The device of claim 11, in which a bipolar transistor of the thyristor that is associated with the first base-emitter junction region comprises a gain (beta) characteristic when under ~~across~~ a low-level bias condition ~~region therefor~~, of magnitude substantially less than an ideal gain characteristic that would otherwise be available therefor absent the lifetime-adjusting defects.

Claim 18 (currently amended): The device of claim 11, in which the base-to-base junction region ~~between the two different base regions of the thyristor~~ is substantially free of the lifetime-adjusting defects.

Claim 19 (currently amended): A semiconductor memory comprising:

an access transistor comprising a gateable channel; and

a capacitively-coupled thyristor memory cell accessible via the access transistor, the capacitively-coupled thyristor comprising:

a cathode/anode region formed in semiconductor material and electrically coupled to a drain/source region of the access transistor,

at least one base-emitter junction region electrically in series with the cathode/anode region, and

leakage species disposed in a region including a portion of a depletion width of the base-emitter junction region.

Claim 20 (original): The device of claim 19, in which the leakage species comprises carbon.

Claim 21 (original): The device of claim 20, in which:

the semiconductor material comprising silicon; and

the leakage species comprises C-Si self-interstitial type complexes.

Claim 22 (original): The device of claim 21, the C-Si self-interstitial type complexes comprising a density sufficient to establish a lifetime for minority carriers within the depletion width of the base-emitter junction region of magnitude substantially less than that for intrinsic silicon.

Claim 23 (original): The device of claim 22, in which the C-Si self-interstitial type complexes form "micro" defects within the silicon lattice associated with the depletion width of the base-emitter junction region.

Claim 24 (original): The device of claim 23, in which the micro defects comprise an average diameter less than one nanometer.

Claim 25 (previously withdrawn). A method of fabricating a semiconductor device, comprising:

implanting dopant into semiconductor material for at least one of anode, N-base, P-base and cathode regions for a thyristor; and

implanting impurities into select regions of the semiconductor material,

the select regions to extend across at least one of a first junction region for between the anode and N-base regions and a third junction region for between the cathode and P-base region.

Claim 26 (previously withdrawn). The method of claim 25, the implanting of impurities to comprise implanting of carbon.

Claim 27 (previously withdrawn). The method of 26, further comprising using a mask over the semiconductor material during the implanting of the carbon to protect a second junction region for between the N-base and P-base regions.

Claim 28 (previously withdrawn). The method of claim 26, further comprising:

annealing the semiconductor material to activate dopant implants, and

annealing the semiconductor material with the implanted carbon across the at least one of the first and third junction regions.

Claim 29 (previously withdrawn). The method of claim 28, in which the annealing to activate and the annealing of the semiconductor material with the implanted carbon share a common anneal.

Claim 30 (previously withdrawn). The method of claim 28, in which at least one of the annealing uses a temperature greater than 600 degrees Celsius and less than 1200 degrees Celsius and a duration less than 20 seconds.

Claim 31 (previously withdrawn). The method of claim 28, in which the implanting of the carbon forms a carbon distribution across each of the first and the third junction regions.

Claim 32 (previously withdrawn). The method of claim 28, in which the implanting of the carbon into the semiconductor material comprises:

using an edge of a mask over the semiconductor material for the alignment of the carbon implant; and

selecting an angle and energy of incidence for the implanting of the carbon to define a lateral extent therefor beneath the mask that is less than that for the N-base region.

Claim 33 (previously withdrawn). The method of claim 32, in which the implanting of the carbon comprises using an angle of incidence therefore relative to the horizontal that is greater than that for the implanting of the N-type dopant and less than 80 degrees.

Claim 34 (previously withdrawn). The method of claim 33, in which an implanting of dopant for the anode comprises:

implanting dopant into the region of the semiconductor material for the anode;

aligning the implanting of the dopant for the anode using the same edge of the mask over the semiconductor material as that for the implanting of the base region; and

selecting an angle of incidence for the implanting between 80 to 100 relative to the surface of the semiconductor material.

Claim 35 (previously withdrawn). The method of claim 34, further comprising using an implant dosage for the carbon greater than about 10^{13} per cm^3.

Claim 36 (previously withdrawn). The method of claim 26, further comprising using a layer of silicon less than 10,000 angstroms over an insulator for the semiconductor material.

Claim 37 (previously withdrawn). The method of claim 26, further comprising selecting parameters for at least one of a density and an anneal for the carbon implants into the semiconductor material sufficient to effect a low-voltage leakage characteristic for the at least one of the first and the third junctions to be substantially greater than the leakage therefor absent the carbon.

Claim 38 (previously withdrawn). The method of claim 37, in which the lower voltage leakage characteristic, over a lower voltage bias region, shall be at least two times greater than a leakage therefor absent the carbon.

Claim 39 (previously withdrawn). The method of claim 26, further comprising selecting at least one of a density and anneal for the carbon implants in the semiconductor material to establish a gain for at least one of the bipolar transistors, across a low-level bias region, of the thyristor to be substantially less than a gain therefor absent the carbon.

Claim 40 (previously withdrawn). The method claim 39, in which the low-level bias region comprises a current range wherein a carbon-effected leakage component of the leakage current dominates the ideal diode diffusion current component.

Claim 41 (previously withdrawn). The method of claim 26, further comprising using a dosage and energy for the carbon implanting to implant the carbon in the select regions of the semiconductor material with a density of at least 10^{17} per cm^3.

Claim 42 (previously withdrawn). The method of claim 41, further comprising using a temperature and a duration for an anneal of the carbon implants sufficient to form defects with an average diameter less than 1 nm.

Claim 43 (previously withdrawn). The method of claim 42, further comprising using a temperature of at least 400 °C for the temperature of anneal of the carbon implants.

Claim 44 (previously withdrawn). A method of processing, comprising:

implanting dopant of first type conductivity into a first select region of a layer of silicon for a base region of a thyristor;

implanting dopant of second type conductivity opposite the first into a second select region of the layer of silicon for an emitter region of the thyristor neighboring the base region; and

implanting adjustment species into a third select region of the layer of silicon overlapping a boundary defined between the base region and the emitter region.

Claim 45 (previously withdrawn). The method of claim 44, the adjustment species comprising carbon.

Claim 46 (previously withdrawn). The method of claim 45, further comprising:

activating the first and second type conductivity dopants implanted in the layer of silicon; and

starting the activating after the implanting of the carbon.

Claim 47 (previously withdrawn). The method of claim 46, in which the activating the dopants comprise annealing the layer of silicon using a temperature of at least 400 degrees Celsius.

Claim 48 (previously withdrawn). The method of claim 46, in which the activating the dopants comprises exposing the layer of silicon to an ambient temperature of between 600-1200 degrees Celsius.

Claim 49 (previously withdrawn). The method of claim 45, in which the implanting the dopant of first type conductivity, the implanting the dopant of second type conductivity and the implanting the carbon each comprise a self-alignment thereof relative to an edge of a common implant mask.

Claim 50 (previously withdrawn). The method of claim 49, further comprising using an angle of incidence for the implanting of the carbon that is between a first angle of incidence for the implanting of the first-type conductivity dopant and a second angle of incidence for the implanting of the second-type conductivity dopant.

Claim 51 (previously withdrawn). The method of claim 45, using a dosage of carbon for the carbon-type implant and an anneal temperature for the activating that are sufficient to effect a minority-carrier lifetime in a depletion region of the boundary.

Claim 52 (previously withdrawn). The method of claim 51, in which the dosage and the anneal temperature are selectant sufficient to effect the minority-carrier lifetime to be less than one-half a lifetime therefore in an intrinsic silicon material.

Claim 53 (previously withdrawn). A method comprising:

operating a capacitively-coupled thyristor memory; and

shunting current of at least a first base region of a thyristor of the capacitively-coupled thyristor memory during the operating.

Claim 54 (previously withdrawn). The method of claim 53, wherein the shunting comprises shunting a low-level current between the first base region and another node.

Claim 55 (previously withdrawn). The method of claim 54, further comprising biasing the another node.

Claim 56 (previously withdrawn). The method of claim 54, wherein the shunting low-level current comprises shunting a low-level current between the first base region and an adjacent emitter region.

Claim 57 (previously withdrawn). The method of claim 54, wherein the shunting low-level current comprises shunting current between the first base region and a contact electrically coupled to an emitter region adjacent to the first base region.

Claim 58 (previously withdrawn). The method of claim 53, in which the operating comprises biasing an electrode capacitively-coupled to a second base region of the capacitively-coupled thyristor.

Claim 59 (previously withdrawn). The method of claim 58, wherein the shunting current comprises shunting a tunneling current to the base region.

Claim 60 (previously withdrawn). The method of claim 59, in which the shunting a tunneling current comprises tunneling charge across a tunneling dielectric.

Claim 61 (previously withdrawn). The method of claim 53, wherein the shunting current comprises passing a low-level current through a resistive path between an emitter region and a base region of an anode end portion of the capacitively-coupled thyristor.

Claim 62 (previously withdrawn). The method of claim 61, further comprising shunting current through a resistive path between an emitter region and a base region of a cathode end portion of the capacitively-coupled thyristor.

Claim 63 (previously withdrawn). The method of claim 53, wherein the shunting current comprises propagating a low-level current through an intervening region between the first base region and the emitter region, the intervening region comprising dopant concentration that is higher than that of the first base region.

Claim 64 (previously withdrawn). The method of claim 63, wherein the shunting current further comprises propagating the low-level current through a depletion region associated with the intervening region.

Claim 65 (previously withdrawn). The method of claim 53, wherein operating the capacitively-coupled thyristor comprises controlling a bias level of an electrode capacitively-coupled to a base region of the thyristor.

Claim 66 (previously cancelled).

Claim 67 (previously amended): A thyristor semiconductor memory device comprising:

a thyristor comprising anode-emitter and cathode-emitter regions and two separate base regions of opposite type conductivity between the anode-emitter region and the cathode-emitter region;

an electrode capacitively-coupled to one of the two base regions; and

a shunt to shunt low-level current of at least one of the base regions, comprising:

a transistor having source and drain regions;

one of the source and drain regions electrically coupled to one of the cathode and anode regions of the thyristor;

the other of the source and drain regions being electrically coupled to one of the two base regions; and

the transistor further comprising a gate electrically coupled to the other of the two base regions and operable under bias to control a conductivity between the source

and drain regions.

Claim 68 (previously cancelled).

Claim 69 (previously cancelled).

Claim 70 (previously withdrawn). A method of manufacturing a semiconductor device comprising:

forming a thyristor with anode-emitter and cathode-emitter regions, and first and second base regions between the anode-emitter region and the cathode-emitter region;

forming an electrode capacitively-coupled to the second base region; and

forming a low-level current shunt to shunt current at a first base region.

Claim 71 (previously withdrawn). The method of claim 70, wherein;

the forming of a thyristor device comprises implanting the first base region with N-type dopant; and

the low-level current shunt is formed between the first base region of N-type dopant and another node that is operable to receive the bias voltage.

Claim 72 (previously withdrawn). The method of claim 70, wherein the forming the low-level current shunt comprises forming a low resistance contact therefor coupled to the anode-emitter region and a relatively higher resistance contact therefor coupled to the first base region.

Claim 73 (previously withdrawn). The method of claim 70, wherein the forming the low-level current shunt comprises forming the current shunt to shunt current between the first base region and the anode-emitter region.

Claim 74 (previously withdrawn). The method of claim 73, further comprising forming one of an intervening region between the anode-emitter and the first base region with a dopant concentration gradient for a substantially enhanced concentration of dopant therefore proximate the other region.

Claim 75 (previously withdrawn). The method of claim 74, the enhanced concentration therefore to impart tunnel-diode characteristics for the junction defined between the anode-emitter and the first base region.

Claim 76 (previously withdrawn). The method of claim 75, wherein the anode-emitter region and the first base region may further define a depletion region therebetween/thereof as a part of the current shunt.

Claim 77 (previously withdrawn). The method of claim 70, wherein the forming the current shunt comprises implanting lifetime adjustment species to affect a minority-carrier lifetime in a region across at least one base-emitter junction for the thyristor.

Claim 78 (previously withdrawn). The method of claim 70, wherein the forming the current shunt comprises;

forming a region having a low effective minority-carrier lifetime across at least one base-emitter junction for the thyristor; and

forming the region for low effective minority-carrier lifetime with at least one of polycrystalline, amorphous and re-crystallized material.

Claim 79 (previously withdrawn). The method of claim 78, wherein the forming the region of low effective minority-carrier lifetime comprises bombarding the region with sufficient energy of bombardment to damage a crystalline structure therein.

Claim 80 (previously withdrawn). The method of claim 77, wherein the implanting the lifetime-adjustment species comprises implanting the region with at least one species of the group consisting of a metal, group IV and group VIII type species of the periodic table.

Claim 81 (previously withdrawn). The method of claim 80, in which the implanting the lifetime-adjustment species comprises implanting the region with carbon.

Claim 82 (currently amended): The semiconductor device of claim 2, in which the carbon within the at least one <u>of the first and the second</u> base-emitter junction <u>regions</u> causes a reduction in a bipolar gain <u>characteristic</u> of the thyristor.

Claim 83 (currently amended): The semiconductor device of claim 82, in which the bipolar gain is dependent on an operable current ~~flows~~ across the at least one of the base-emitter junction regions and the reduction in gain is greater at lower ~~current~~ levels of current than at higher ~~current~~ levels.

Claim 84 (previously added): The semiconductor device of claim 67, in which:

the transistor comprises a MOSFET;

the source/drain region of the MOSFET electrically coupled to the cathode region of the thyristor;

the drain/source region of the MOSFET electrically coupled to the p-base region of the thyristor; and

the gate of the MOSFET electrically coupled to the n-base region of the thyristor.

Claim 85 (previously added): The semiconductor device of claim 67, in which:

the transistor comprises a MOSFET defined in part by the source region, the drain region and the gate;

the drain/source region of the MOSFET electrically coupled to the anode region of the thyristor;

the source/drain region of the MOSFET electrically coupled to the n-base region of the thyristor; and

the gate of the MOSFET electrically coupled to p-base region of the thyristor.